All India Council for Technical Education

Nelson Mandela Marg, VasantKunj, New Delhi-110070

Hardware Challenge using स्वदेशी Microprocessors

एक कदम #आत्मनिर्भरता की ओर from 15th August 2020

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Sir / Madam,

Greetings from All India Council for Technical Education!

It is pleased to inform you that, inspired by the government's #Atma Nirbhar Bharat Vision, the Ministry of Electronics and Information Technology (MeitY) has announced the Hardware Challenge under Microprocessor Development Programme, in consultation with the participating institutions i.e. C-DAC, IIT Madras & IIT Bombay. This is as a step towards achieving the self-reliance in the hardware domain with the following broad contours:

1. Hardware Challenge using स्वदेशी Microprocessors has been announced on 15th August 2020 for an overall duration of 10 months with a total award amount of Rs. 4.30 Crore earmarked in different phases, to inculcate the culture of taking up the complex designs in the country around indigenous processors of C-DAC (VEGA processors) & IIT Madras (SHAKTI processors).

2. Participation in proposed Hardware Challenge: Will be sought not only from engineering college students (B.Tech/ M.Tech/ PhD level) but also from the Start-ups working in this area, in line with the objective of achieving a horizontal spread of this technology. All efforts will be made to disseminate the information & reach out to masses and involve the participation of all stakeholders in this Challenge.

3. Roadmap for engaging stakeholders & information dissemination: Respective websites of C-DAC (http://vegaprocessors.in/hwchallenge.html) & IIT Madras (https://shakti.org.in/gc2020-shakti.html) have already been developed for providing information on Embedded / Controller class of SHAKTI/ VEGA processors & associated Hw/ Sw ported on Xilinx FPGA Boards.

4. The other detailed information on the proposed Hardware Challenge as Background Note (like- Stages of Challenge, Award amount, roles & responsibility, etc) is attached herewith. For more information, please visit: http://vegaprocessors.in/hwchallenge.html, https://shakti.org.in/gc2020-shakti.html

Through this Challenge, the efforts are being made to touch base with all young innovators/ entrepreneurs and facilitate them tinkering with our Swadeshi Processors and also let them innovate the frugal solutions for societal issues. In view of the above, you are requested to kindly disseminate this information among faculty members and students (current & pass-outs both) as a step towards achieving the self-reliance in the hardware domain in the country.

Best Regards,
AICTE, New Delhi

Hardware Challenge using स्वदेशी Microprocessors

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Stakeholders: Following are the various stakeholders of the proposed Challenge:

#	Stakeholder	Details
1	**Eligible Participants**	**(a) Indian students** pursuing undergraduate, postgraduate & Doctoral degrees with Indian engineering colleges. Teams of not more than 5 students and 2 faculty members. **(b) Start-ups**
2	**Technology Providers**	**(a) IIT Madras**: Selected processor variants of शक्ति processor family (32-bit E-Class and 64-bit C-Class variants) have been made available on Open web-portal at https://shakti.org.in/ **(b) C-DAC:** Selected processor variants of वेगा processor family (Thejas-32 and Thejas-64 variants) is being made available on Open web-portal at http://www.vegaprocessor.in/ **(c) MyGov portal** is being made available to applicants for Challenge Registration and wider outreach, which will be redirecting the applicants to the respective processors websites of IIT Madras & C-DAC. **(d) Xilinx** has donated 100 FPGA Hw Boards free-of-cost for Semi Finalists in the proposed Challenge for porting the processors & associated ecosystem on them. It may kindly be noted that not only the processor variants but also the entire associated Hw/ Sw ecosystem is being made available for these processors (Software Development Kit, Tool Chain, ports of OS/ FPGA, Tutorials , demo applications etc) on their respective web-portals.
3	**Incubation Centre(s)**	Following are the broad activities to be carried out by the Maker Village, Kochi as the identified Incubation Centre(s): (i) During the duration of Hardware Challenge: (a) Coordination of various Technical, Financial & Administrative activities including finalizing the review process, evaluation of Applications etc. (b) Facilitating regular technical guidance & mentoring applicants in collaboration with C-DAC, IIT Madras & other experts. (ii) 12-month support subsequent to the Final Phase of Hardware Challenge for: (a) Incubating the Start-ups and provide requisite support for fostering an innovation mindset and enabling networking with industry peers/ VCs. (b) Monitor the progress of incubated start-ups for next 12 month and make milestones linked fund releases to them.
4	**Technical, Business & Incubation expertise**	Technical experts from Incubation Centres, Academia, Industry, Industry Associations and Technology providers (C-DAC, IIT Madras, Xilinx etc.) are being involved in various Committees at different Phases of the Challenge (Quarter Finals, Semi Finals, Finals & further) for not only during review process but also for - Application Areas identification, providing guidance to the applicants for technical & business aspects of innovative solutions around processors, incubating the start-ups etc.

Challenge Phases: The details of 4 main Phases of the proposed Challenge (Registration, Quarter Finals, Semi Finals & Finals) in addition to other Phases is as below:

#	Stages	Timeline	Activities & Prize amount
1	**Pre-registration (T0)**	**T0** (Upto Challenge Launch, let say 15/08/2020)	(i) **MyGov**: web-portal is being used for registration & proliferation of information at https://innovate.mygov.in/ by 15th August 2020. (ii) **IIT Madras**: has made available dedicated web portal for providing information on SHAKTI processors & associated Hw/ Sw for Challenge participants at http://vegaprocessors.in/hwchallenge.html (iii) **C-DAC:** has made available dedicated web portal for providing information on VEGA processors & associated Hw/ Sw for Challenge participants at http://vegaprocessors.in/hwchallenge.html
2	**Registration (T1)**	**T0 + 1 month** (let say 15/08/2020 - 15/09/2020	All Applicants meeting the Eligibility Criteria are expected to register on or before 15th September 2020. Teams completing the registration process will enter to the Quarter Finals Phase.
3	**Quarter Finals (T2)**	**T1 + 1 month 25 days** (let say 16/09/2020 - 10/11/2020)	**A. Pre-Screening Stage** (i) Participating students to get approval from Faculty Mentor(s) from their respective College. (ii) Understand the technical details by going through the Video Tutorials made available by IIT Madras and C-DAC (for SDK, FPGA Boards, demo applications etc.) (iii) Answering a Quiz based on these details to ensure that participant has fair knowledge. (iv) Submit the tentative Abstract of the proposal by 10th October 2020 within 1000 words in prescribed format. **B. Ideate Stage** (v) Submit the detailed Proposal by 10th November 2020 on the technology to be implemented in prescribed Proforma.
4	**Preparation Time-1 (T3)**	**T2 + 1 month 20 days** (let say 11/11/20 – 31/12/20)	The Proposals will be reviewed by Domain Experts against 2 categories – Business Potential and Technical Innovation. (i) The announcement for the 100 Teams (50 teams for applications around Arty 35T and 50 teams for applications around Arty 100T) to be shortlisted for the Semi Finals will be made by 25/12/20. (ii) Shipping Xilinx FPGAs to Semi-Finalists before 31/12/2020.
5	**Semi Finals (T4)**	**T3 + 2.5 month** (let say 01/01/2021 - 15/03/2021)	100 Semi Finalists would be asked to register a Start-up in the identified incubation Centre(s) and go through following steps: **A. Minimum Viable Prototype (MVP) Stage** (i) Total 1st installment of Cash Prize of Rs. 25.00 Lakh to 100 Semi Finalists (Rs. 25,000 to each team) and access to Indigenous Processor Ecosystem & Xilinx Board may be made available to them. This Cash Prize may also be used by them to procure the commercial off-the-shelf COTS) components to develop MVP. (ii) The monthly progress to be submitted along with following- Progress Report including deviations, if any and Video demonstration of MVP & Business Plan.
			B. Proof-of-Concept (POC) Stage

			Based on the recommendation by Technical Advisory Committee, total 2nd installment of Rs. 75.00 Lakh of Cash Prize (Upto Rs. 75,000 to each team) may be provided to only those Semi Finalists, who – (a) either demonstrate POC/ substantial progress during the 1st review or, (b) require additional COTS to demonstrate a POC. This Cash Prize may also be used by them to procure the additional COTS to demonstrate the POC.
6	**Preparation Time-2** **(T5)**	**T4 + 0.5 month** (let say 16/03/2021 - 31/03/2021)	The MVP/ POC will be reviewed by a committee comprising of Domain Experts against 2 categories – Business Potential and Technical Innovation. The announcement for the 25 Teams selected for the Finals will be made by 31st March 2021 and provided with the recommendations to improvise further on Technical & Business viability to develop the Hw Prototype.
7	**Final** **(T6)**	**T5 + 2.5 month** (let say 01/04/2021 - 15/06/2021)	**Hardware Prototype Stage** (i) 25 Finalists to be provided with the total Cash Prize of Rs. 1.00 Crore (Rs. 4.00 Lakh to each Team) and Silver Certificate. This Cash Prize may also be used by them to procure the additional COTS to develop the Hw prototype. (ii) The monthly progress to be submitted along with following- Progress Report including deviations, if any and Video demonstration of Hw Prototype & Business Plan. (iii) 25 Finalists will be invited to demonstrate their Hw Prototype in the Final Evaluation event on 15th June 2021.
			Winners Top 10 Teams winning in the Final Stage will be announced in June 2021 for the following awards & support towards incubating their Start-ups at Maker Village, Kochi (a) Gold Certificate. (b) Rs. 35.00 Lakh each to the Winning Team, Rs. 30.00 Lakh to 1st Runner-up Team & Rs. 25.00 Lakh to 2nd Runner-up Team and total Rs. 1.40 Crore to 7 other Teams.

Subsequent to the Final Stage of the Hardware Challenge, it is proposed that the Maker Village, Kochi will incubate the Teams winning in Finals as Start-ups to provide the requisite trainings, technical & business guidance and also extend technology support to them in terms of facilities available at Incubation Centre(s), for translating their technologies. Quarterly reviews will be facilitated by Maker Village for monitoring the progress of incubated Start-ups for next 12 month and Milestones linked fund releases will be made to them.

Evaluation mechanism and Review parameters

3-tier evaluation mechanism: It is proposed that at least a 3-tier process may be adopted for evaluating the proposals/ Hw Prototypes of the participants during each Phase of the Challenge (Quarter Finals, Semi Finals & Finals), which may include the- (a) Initial review to be facilitated by Incubation Centre(s), through the Screening Committee(s) consisting of experts from C-DAC, IIT Madras, Incubation Centre(s), VCs etc., (b) Further review by the TAC (Technical Advisory Committee) constituted by MeitY consisting of experts from Academia, Industry & Industry Associations, (c) Final Decision by JURY panel.

Review Parameters: All proposals & Hw prototypes from the applicants envisioning use of indigenous processors, will be reviewed on technical & business aspects, to be identified in close consultation with all stakeholders including based on the review parameters to be identified primarily on following aspects:

(a) **Approach towards Problem Solving** (Vision, USP & Novelty of Approach)

(b) **Prototype Attributes** (Cost Effectiveness, Scalability, Interoperability, Usability, Underlying technology components/ COTS, etc)

(c) **Roadmap for translation of technology** (Business Opportunity, go-to Market Strategy etc.)

Phase-wise Financial requirement for the proposed Challenge

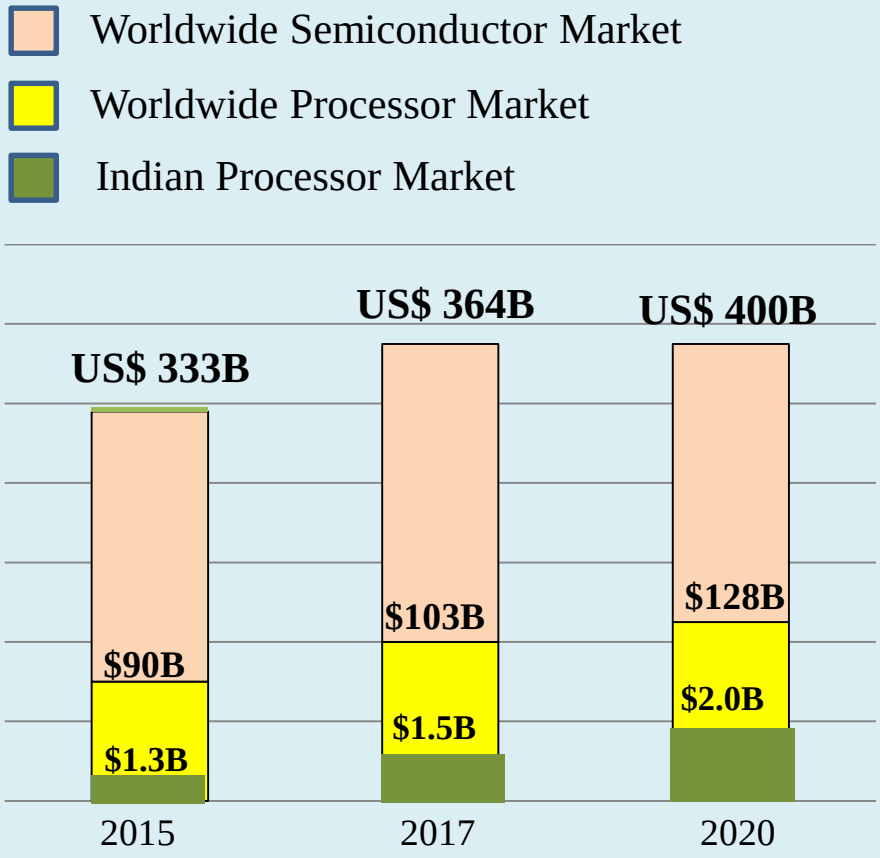
It may kindly be noted that Rs. 500.00 Lakh is proposed as the total expenditure for the Hardware Challenge as per the following break-up vis-à-vis timelines, which will be released to the Maker Village which in turn, will – (a) disburse the Award amount to the partcipants of the Chalenege at various Phases and (b) also incur the expediture for coordination of various Technical, Financial & Administrative activities:

(Rs in Lakh)

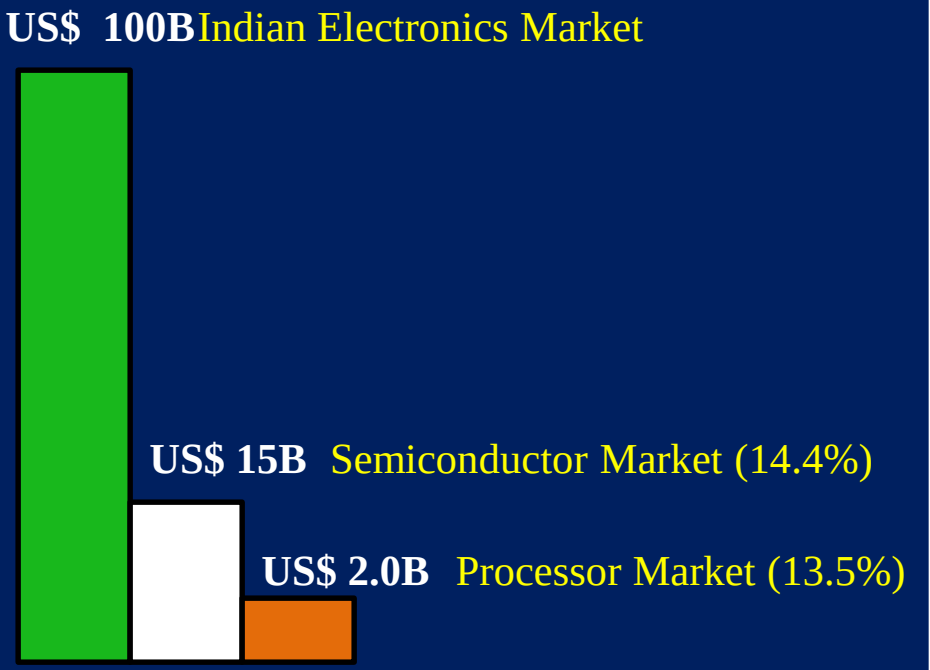
#	Heads	Phase	# of Participants	Award to each Participant	Timeline	Total
1	**Awards**	**(i) Quarter Final**	Open to all Eligible applicants with Indian Nationality	NIL	16/09/2020 - 10/11/2020 (assuming T0 as 15/08/2020)	
		(ii) Semi Final	100	1.00	01/01/2021 - 15/03/2021	**100.00**
		(iii) Final	25	4.00	01/04/2021 - 15/06/2021	**100.00**
		(iv) Winners	10	Award amount and support towards incubating start-ups at identified Incubations Center(s) of (a) Rs. 35.00 Lakh each to the Winning Team, (b) Rs. 30.00 Lakh to 1st Runner-up Team & (c) Rs. 25.00 Lakh to 2nd Runner-up Team and (d) total Rs. 1.40 Crore to 7 other Teams.	June 2021	**230.00**
			Total Award amount			**430.00**
2	**Technical, Financial & Administrative activities**, (a) during the Hardware Challenge and (b) 12-month after the Hardware Challenge, by the Maker Village	--	--	--	September 2020- June 2021	**70.00**
			Grand Total			**500.00**

Microprocessor Market

> 70% of Chips contain Microprocessors !!



Major Players: Intel and AMD, ARM(arch)



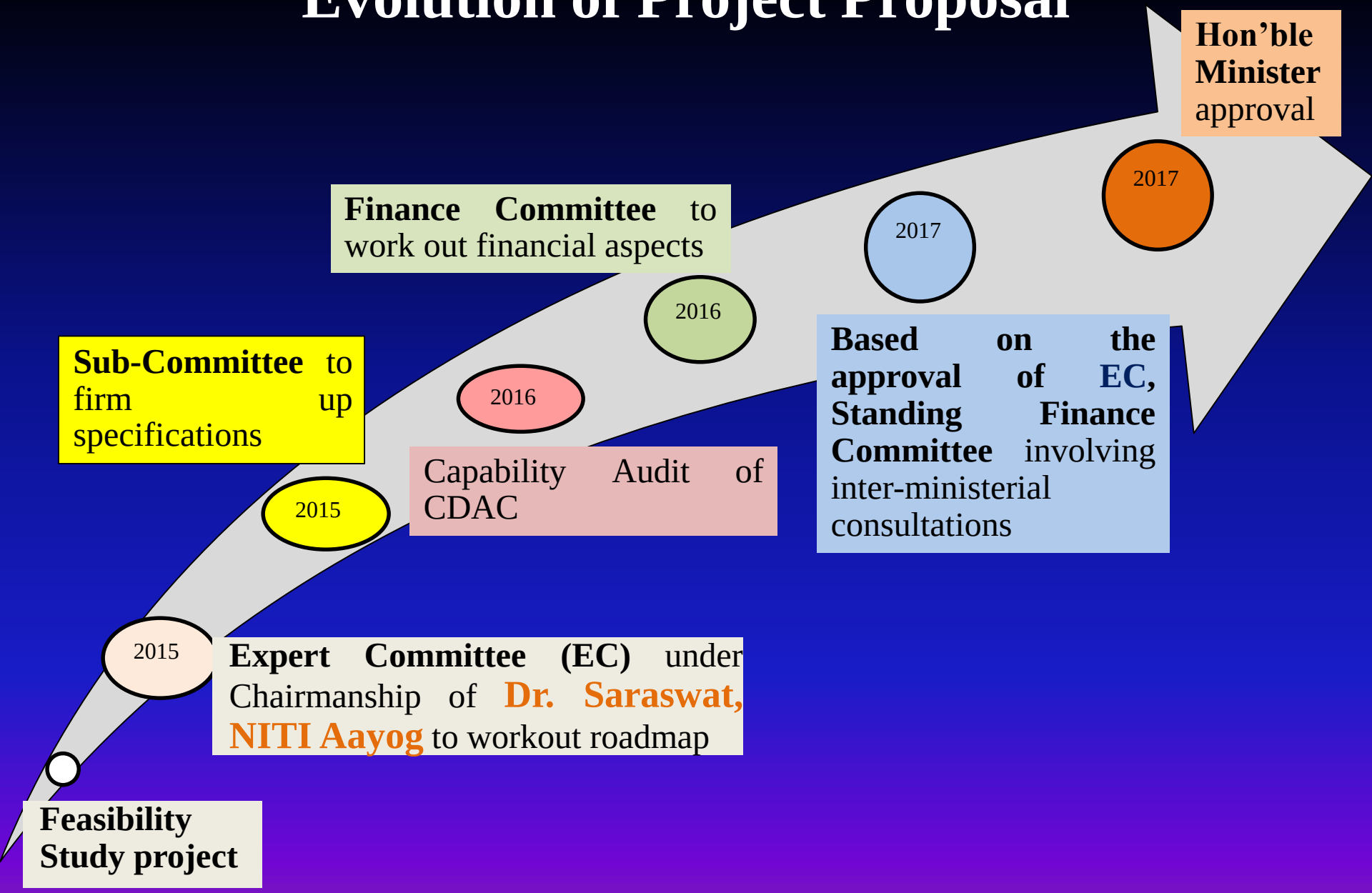
Need for Indigenous Microprocessor

1. Addresses Security aspects
2. Avoid- FE outflow (licensing fee/ recurring royalty)
3. Arbitrary licensing restriction
4. Meet India's strategic/ commercial/ industrial requirement

Microprocessor Development- Indigenous Initiatives

DRDO	1997	ANUPAMA	32-bit @ 33 MHz
	2004	ABACUS	32-bit @ 80 MHz
	2009	MIGACore	32-bit @ 1 GHz
	2009	ABACUS-SOC-Flash	32-bit @ 200 MHz (2 cores)
VSSC	2015	VIKRAM 1601	16-bit @ 30 MHz/ 64 MHz, in-house ISA- in house
BEL	2016	BEL SoC	64-bit @ 1.0-1.2GHz, ARMv7 ISA (4 Cores)
C-DAC	2001	SAMAGRA	8-bit microcontroller
	2004		32-bit, RISC ISA
IIT Bombay	2015	AJIT	32-bit processor @ 300 MIPS, SPARC ISA (jointly funded by MeitY & Powai Labs)
IIT Madras	2015	SHAKTI	64-bit core developed for DRDO (MIPS based ISA)
			Exploring RISCV-ISA based designs

Evolution of Project Proposal



Microprocessor Development Programme

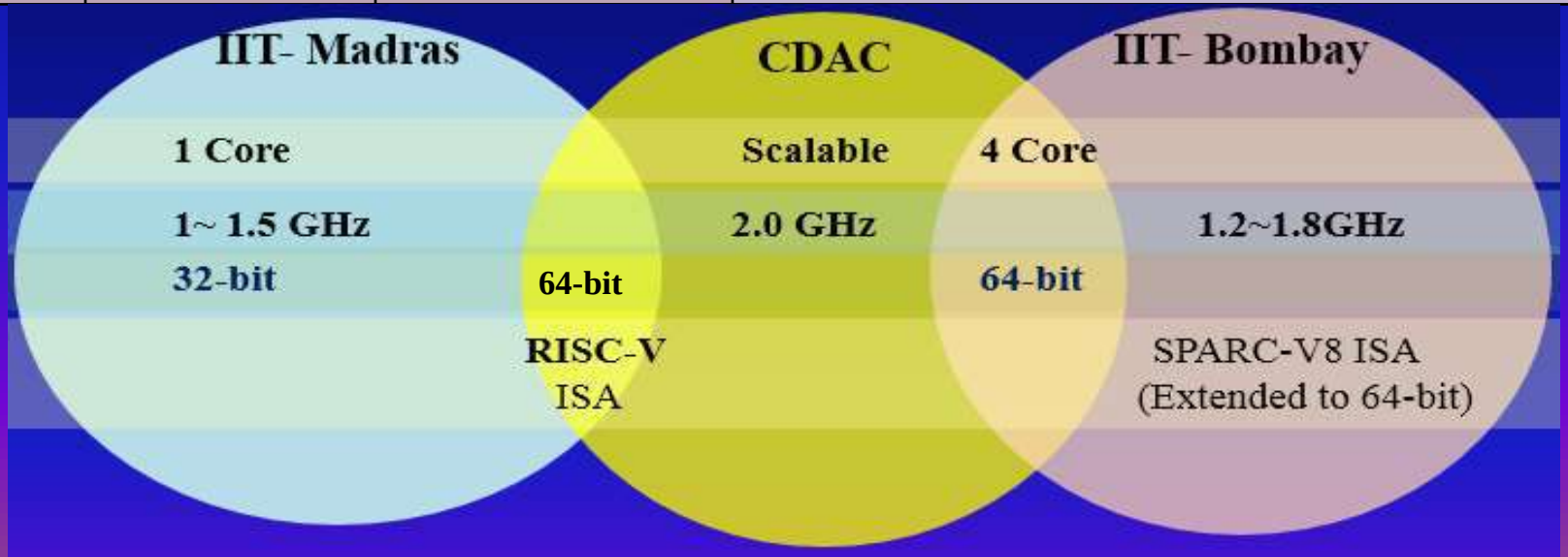
Outlay: **Rs. 289.21 Crore**

Duration: **4 years**

Objectives:

- Development of family of 32/ 64-bit, Quad-Core (upward scalable) microprocessors operating up to 2 GHz using open source ISA & demonstration for identified applications.
- Development of reusable peripheral IP cores & S/w tool-chain for processors.
- Develop capabilities to take up complex designs in Microprocessor & related areas in the country.

	Outlay (in Cr)	**Duration** (in years)	**Applications**
CDAC	**273. 26**	**4**	Energy Meter/Set-top Box/Network Router/ Smartphone
IIT-M	**11.15**	**2**	Secure ID / Network Router/ Other applications
IIT-B	**3.47**	**3**	Secure Network Router



Project Achievements- IIT Madras (under MDP) & IIT Bombay (under NavIC project)

64-bit by IIT-M @ 180nm, SCL

64-bit by IIT-M @ 22nm, Intel

32-bit by IIT-B@ 180nm, SCL

Specifications	IIT Madras		IIT Bombay
Technology Node	22nm, Intel	180nm, SCL	
Frequency	350 MHz	70 MHz	60 MHz
Number of Cores	Single Core		
Design architecture	64-bit		32-bit
ISA	RISC-V		SPARC-V8
Core Power	20mW	400mW	600mW
Die Area	4x4 mm^2	12x12mm^2	7.5x7.5mm^2
Pipelining	5-stage		7-stage

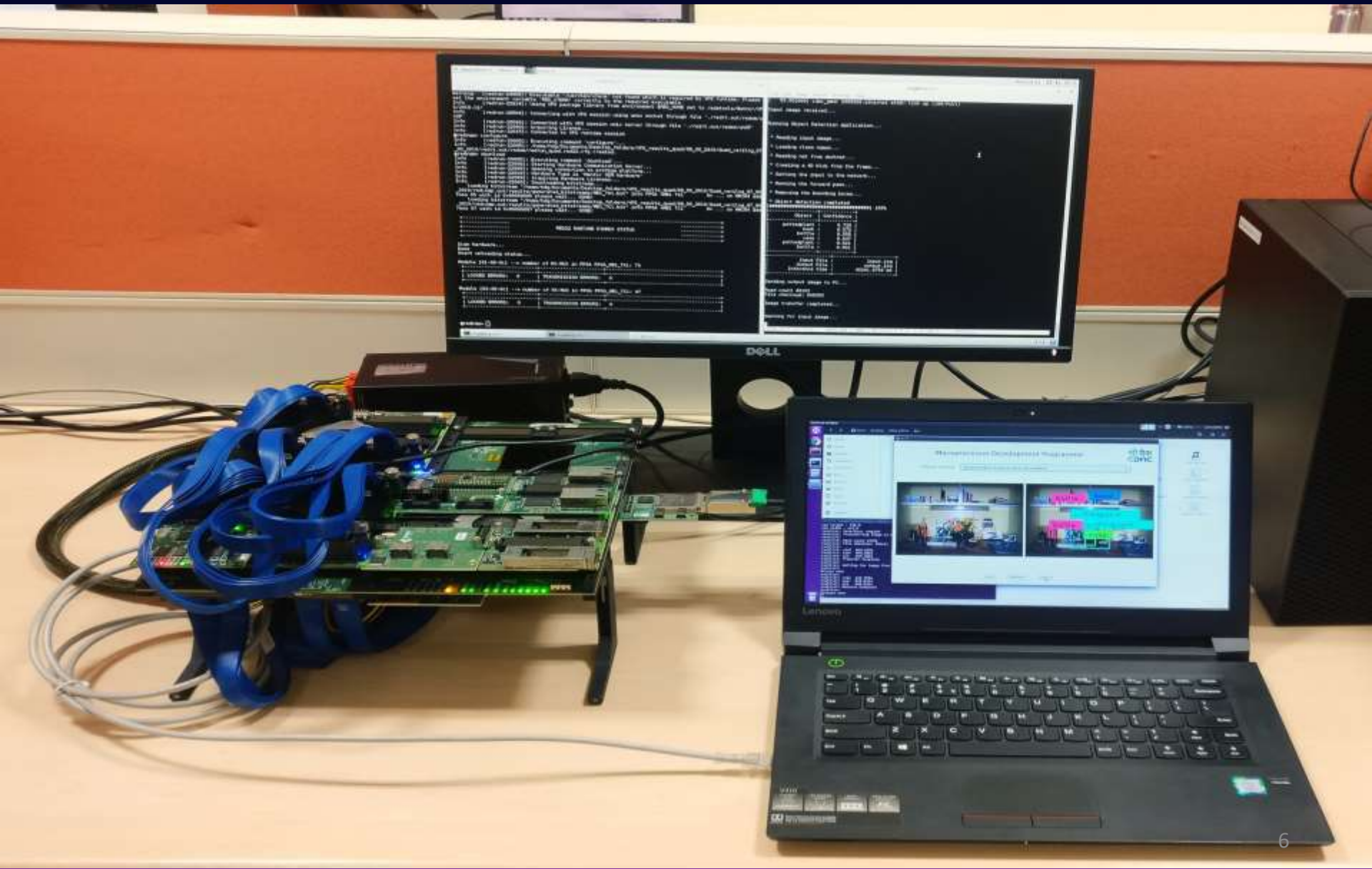
Interested End Users:

1. NPCIL, BARC & IGCAR
2. Accord & BEL for NavIC
3. ISRO/DDP funding further dev.
4. Western Digital, Rezonent & Thales Corporation.

Roadmap ahead

1. Server class Processor proposal
2. Incubated IncoreSemiconductor
3. Study material & Arduino Boards being prepared.
4. Awareness/ training Workshops

Project Achievements- C-DAC Quad core demonstration on FPGA



Thank You